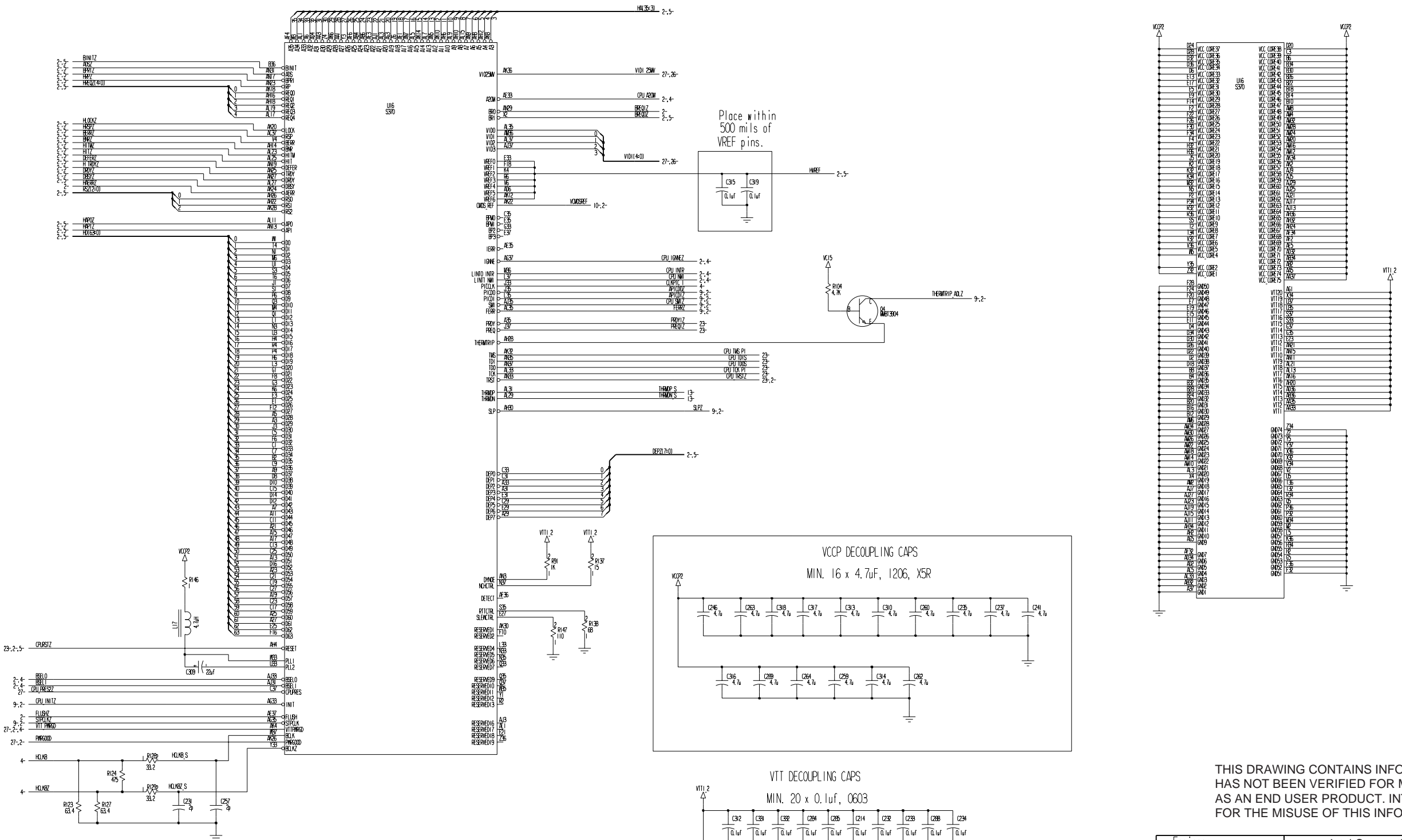




SECONDARY CPU



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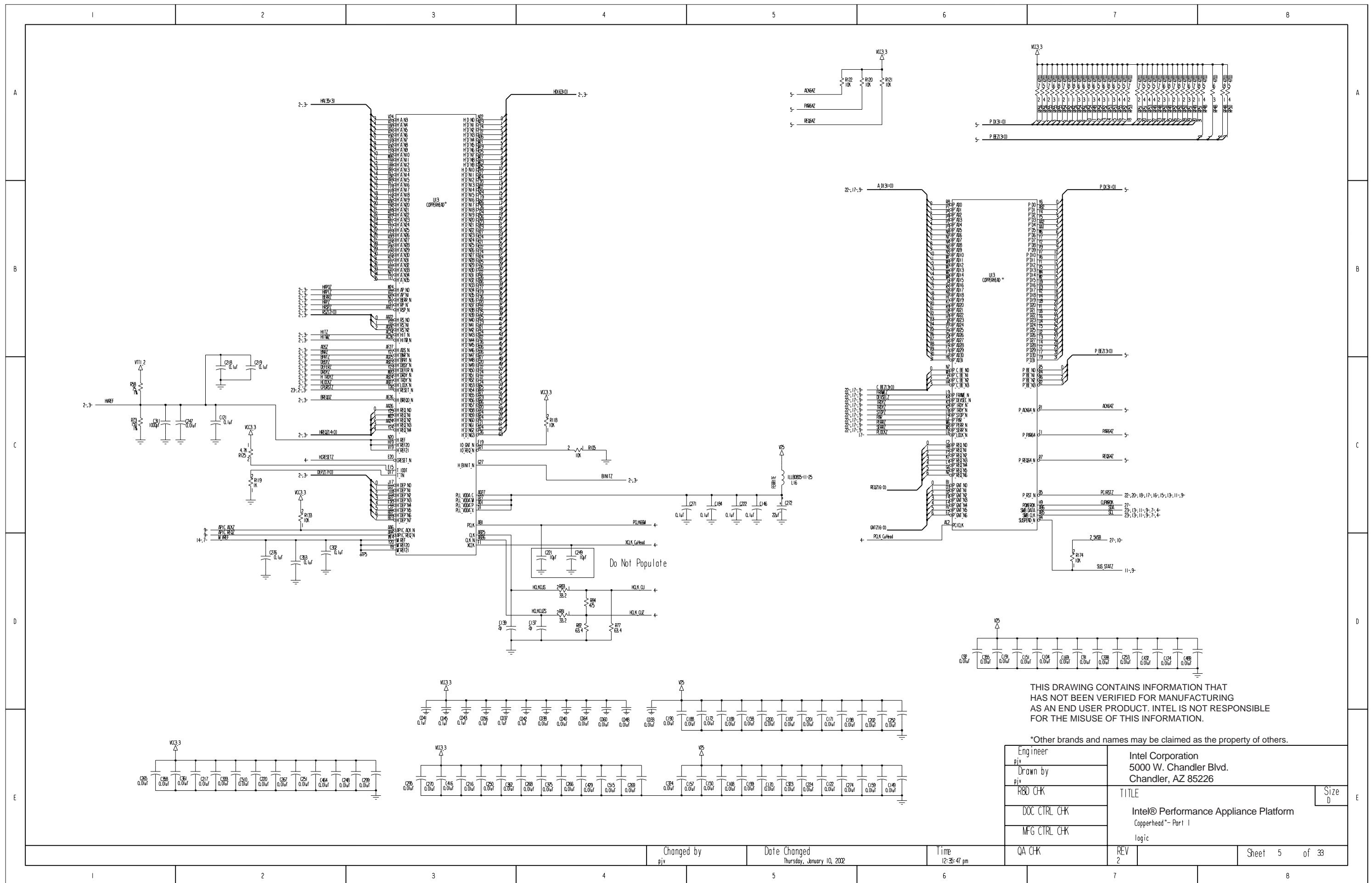
Engineer piv	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by piv			
R&D CHK	TITLE Intel® Performance Appliance Platform Secondary CPU logic		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2	Sheet 3 of 33	

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piv

Date Changed  
Thursday, January 10, 2002

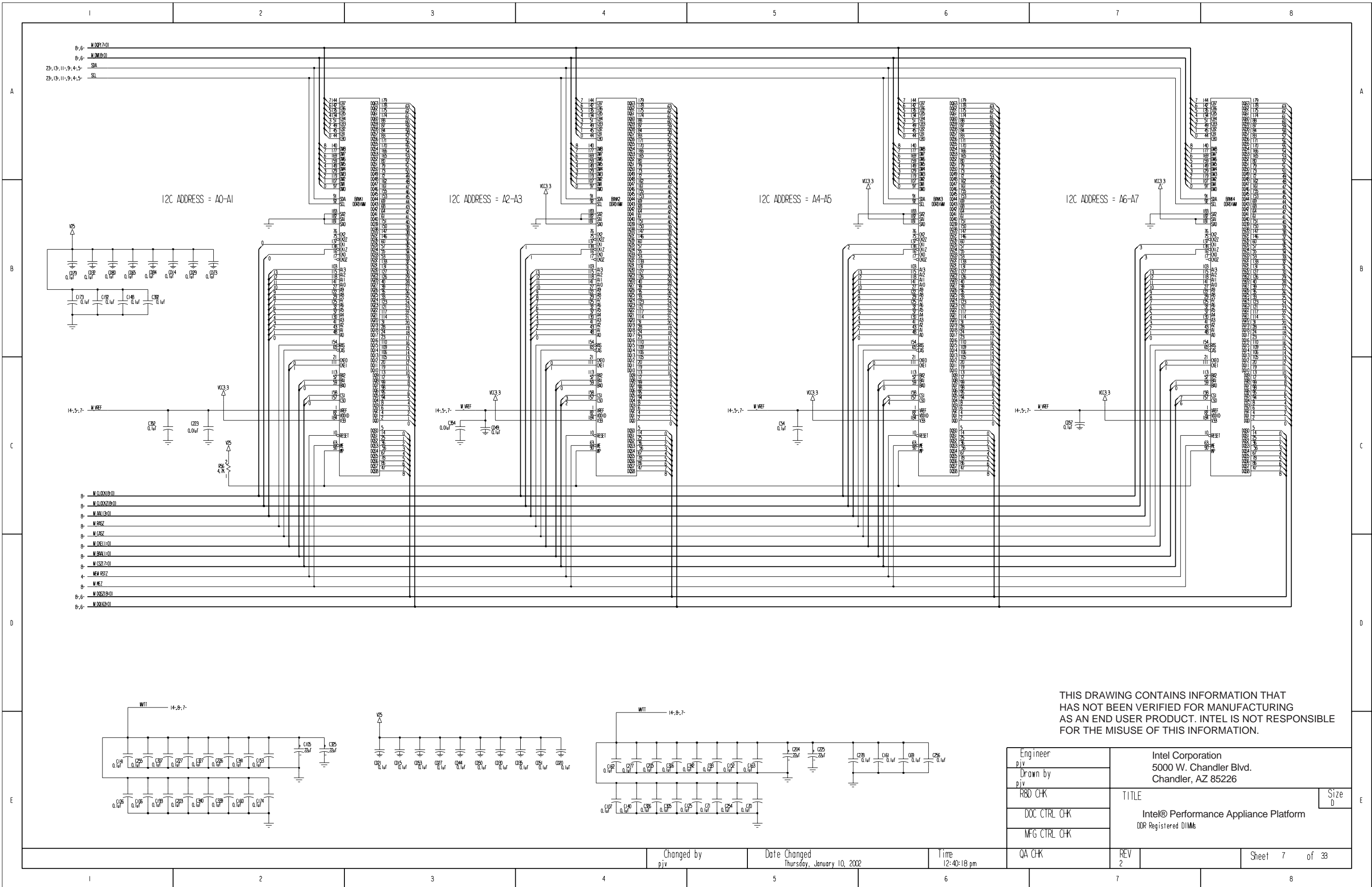
Time  
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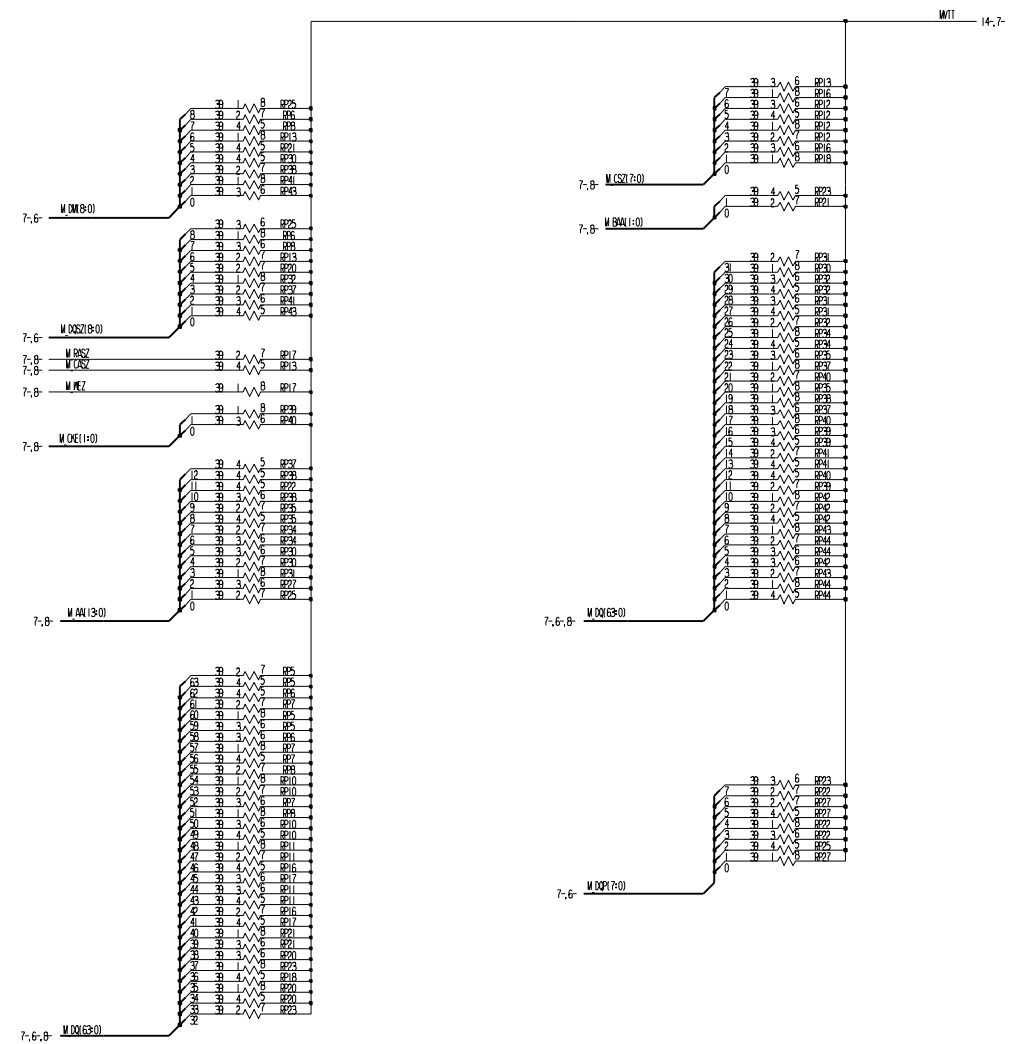
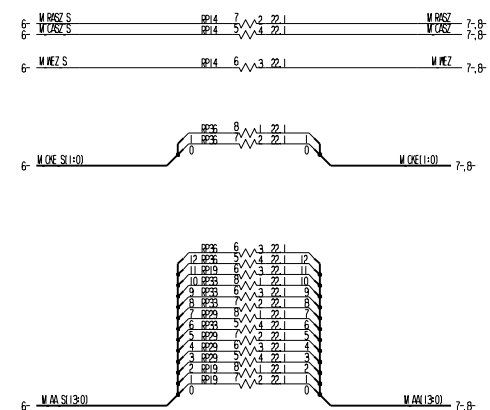
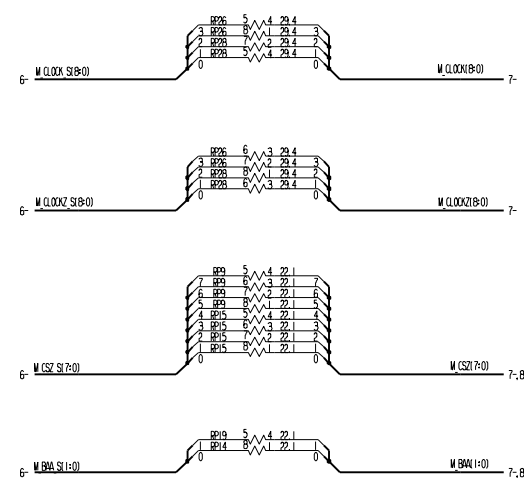






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Engineer p.j.v	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v			
R&D CHK	TITLE Intel® Performance Appliance Platform DDR Registered DIMMs		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2	Sheet 7	of 33

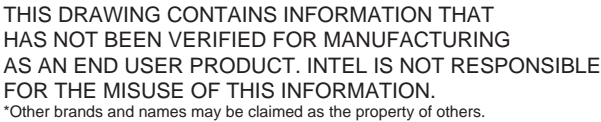


39 2 7 RP18

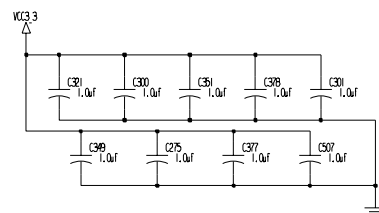
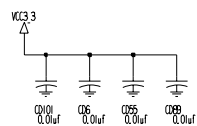
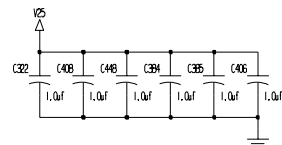
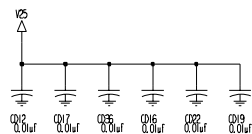
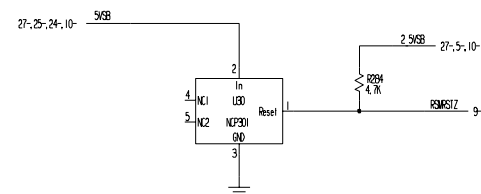
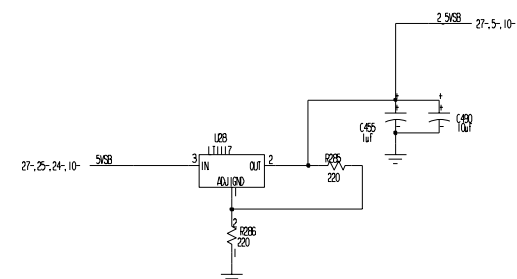
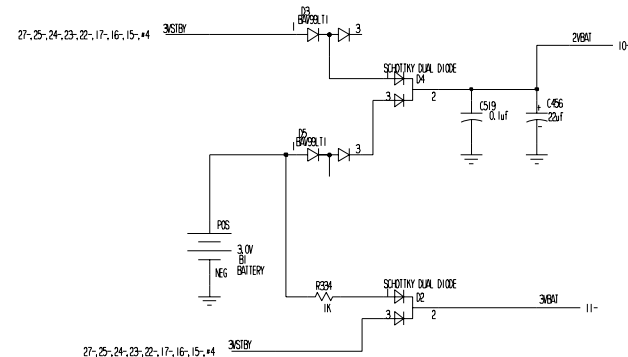
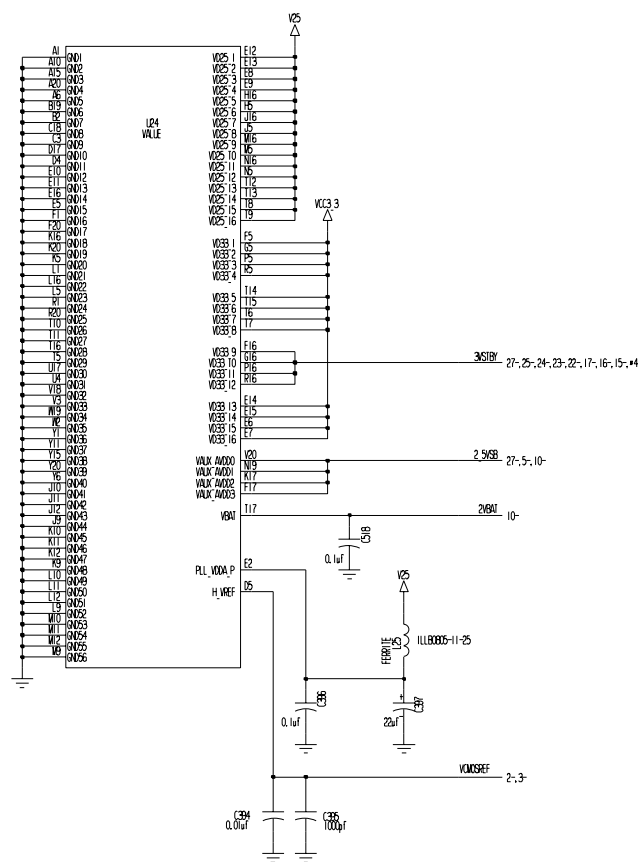
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Engineer bjv	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by bjv			
R&D CHK	TITLE  Intel® Performance Appliance Platform DDR DIMM Termination		Size B
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2		Sheet 8 of 33





Changed by pjv	Date Changed Thursday, January 10, 2002	Time 12:41:47 pm
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\*Other brands and names may be claimed as the property of others.

Engineer p/jv	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p/jv			
R&D CHK	TITLE		Size D
DOC CTRL CHK	Intel® Performance Appliance Platform Coppertail™ Power		
MFG CTRL CHK			
QA CHK	REV 2		Sheet 10 of 33

I/O Base Address  
Set to 0x04E

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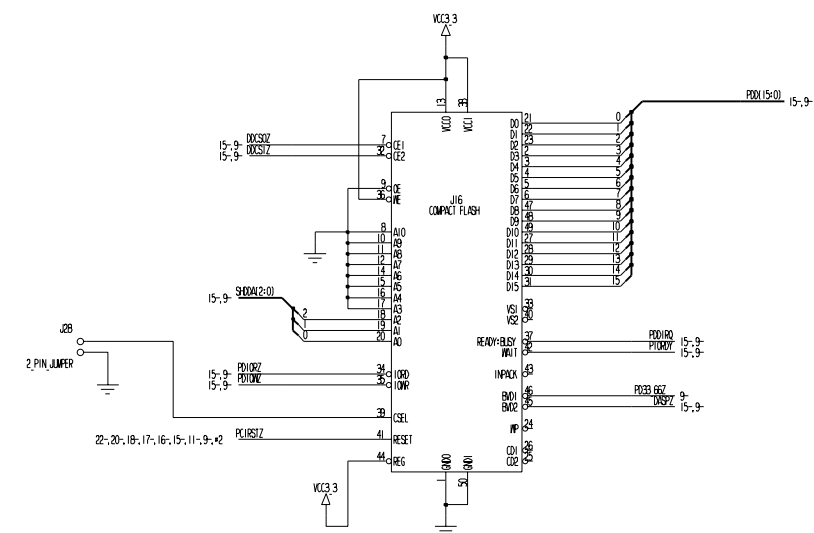
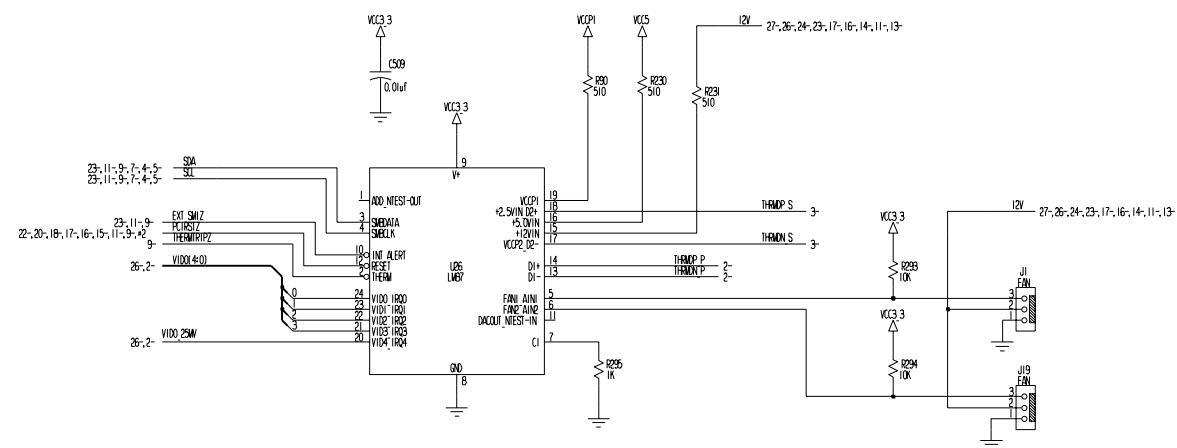
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Drawn by p.j.v			
R&D CHK	TITLE		Size D
DOC CTRL CHK	Intel® Performance Appliance Platform SUPER I/O		
MFG CTRL CHK			
QA CHK	REV 2		Sheet 11 of 33

Changed by  
p.j.v

Date Changed  
Thursday, January 10, 2002

Time  
12:50:21 pm

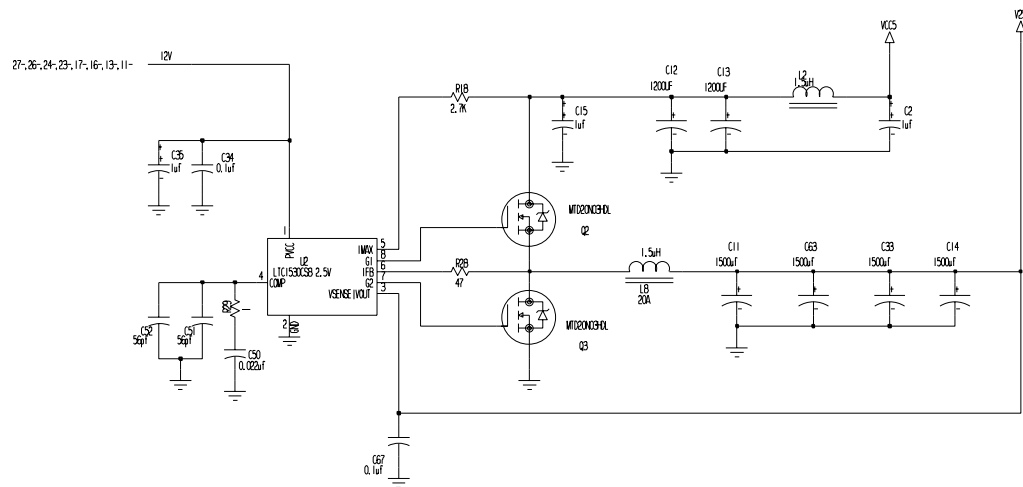
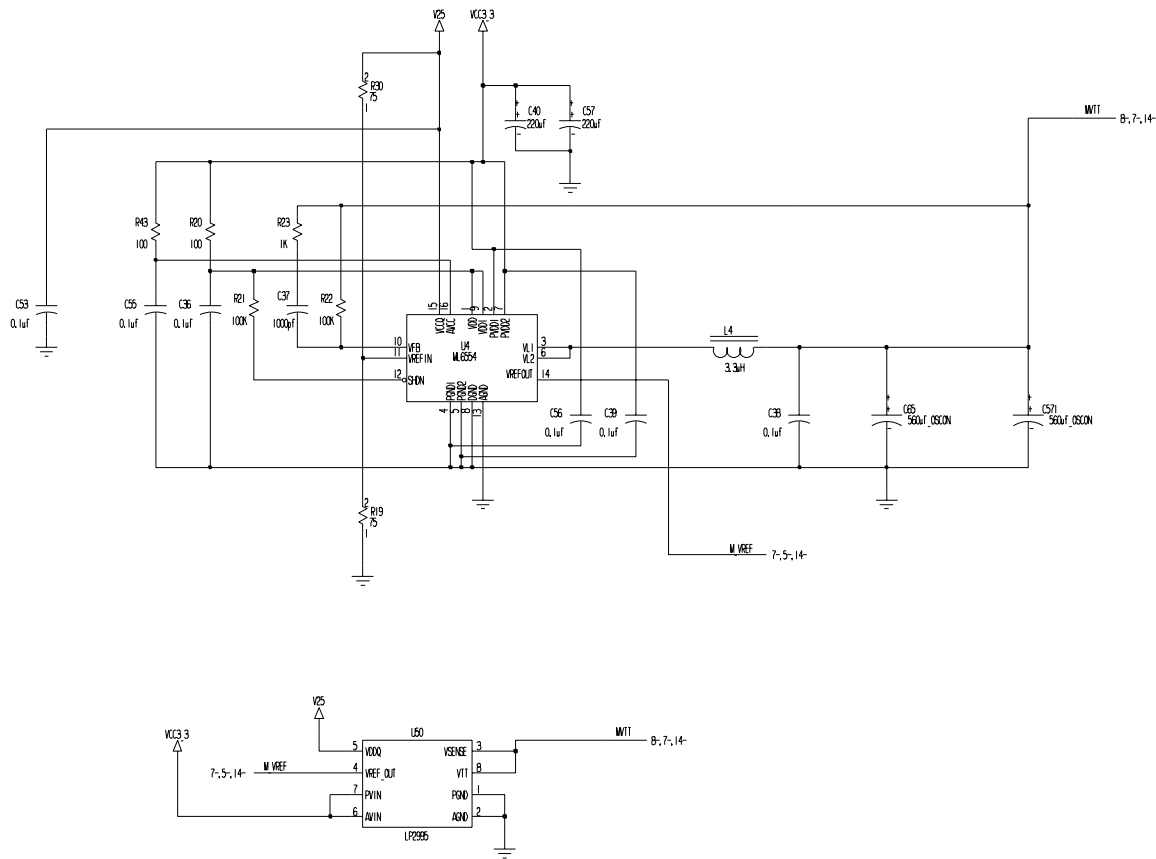




J28	<p>Master/Slave Jumper for Compact Flash</p> <p>Jumper ON = MASTER DEVICE Jumper OFF = SLAVE DEVICE</p>
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Engineer p/jv	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p/jv			
R&D CHK	TITLE		Size D
DOC CTRL CHK	Intel® Performance Appliance Platform		
MFG CTRL CHK	Hardware Monitor & Compact Flash		
QA CHK	REV 2		Sheet 13 of 33



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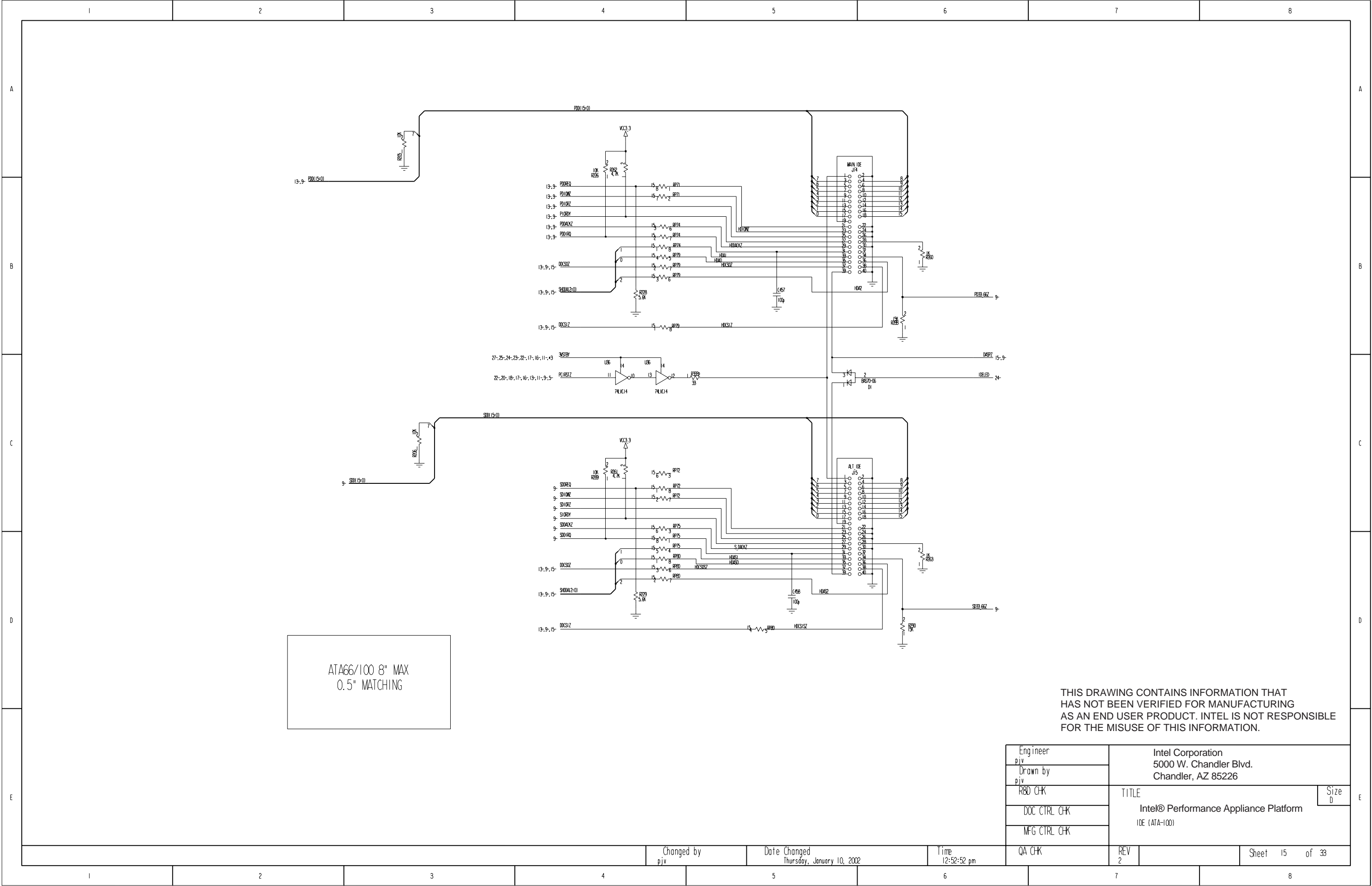
Engineer p.j.v	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v			
R&D CHK	TITLE Intel® Performance Appliance Platform 2.5V Core & SSTL2 Termination Voltage		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2	Sheet 14 of 33	

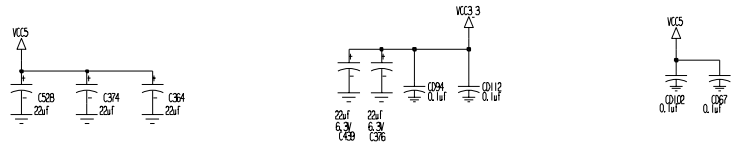
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Date Changed  
Thursday, January 10, 2002

Time  
12:52:19 pm

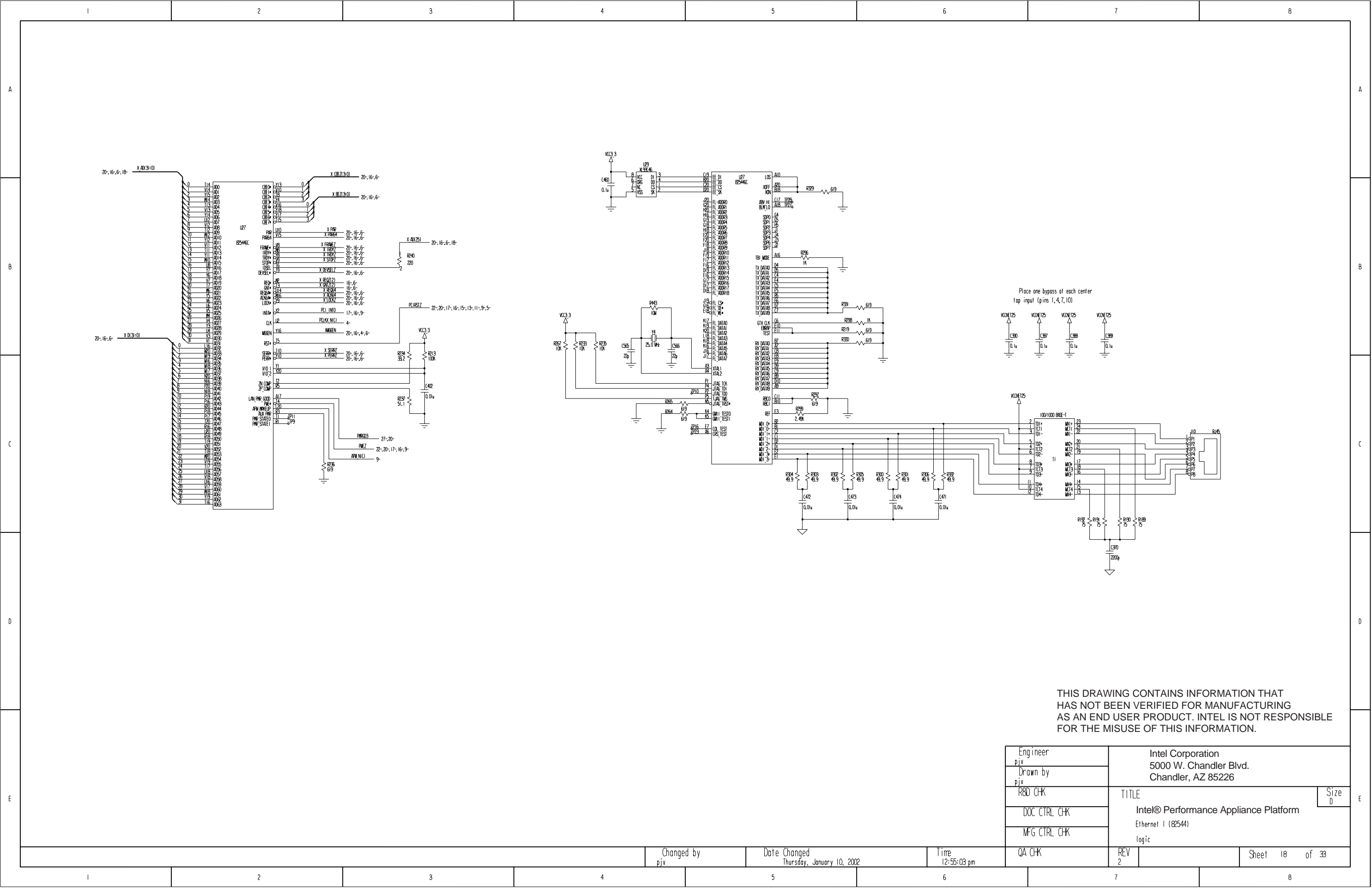






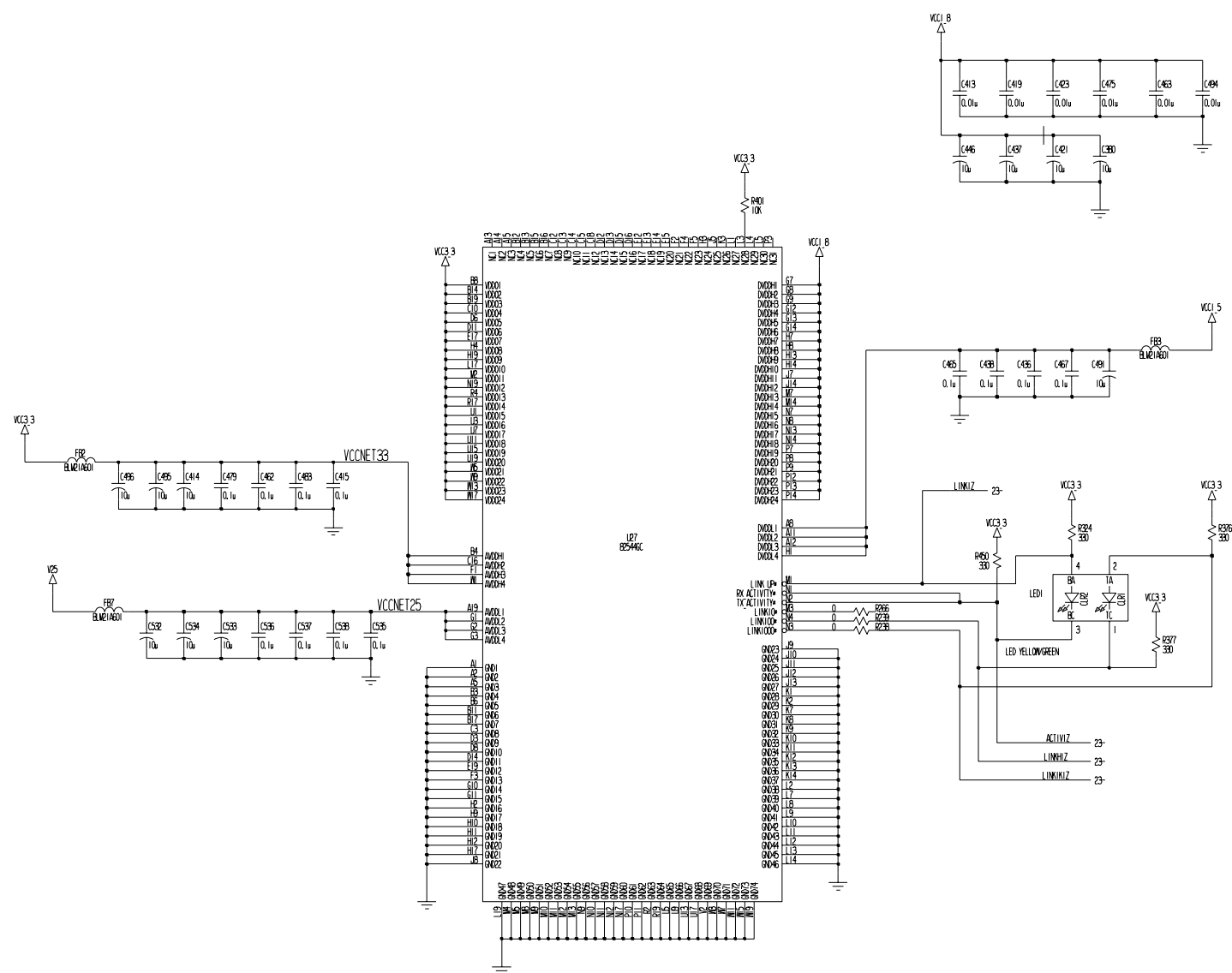
Engineer p.j.v.	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v.			
R80 CHK	TITLE  Intel® Performance Appliance Platform PCI-X Connector		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2		Sheet 16 of 33





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Engineer piv	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by piv			
RED CHK	TITLE Intel® Performance Appliance Platform Ethernet I (82544) logic		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2	Sheet 18 of 33	



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Engineer p.j.v.	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v.			
R&D CHK	TITLE Intel® Performance Appliance Platform Ethernet I - Power		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2	Sheet 19 of 33	

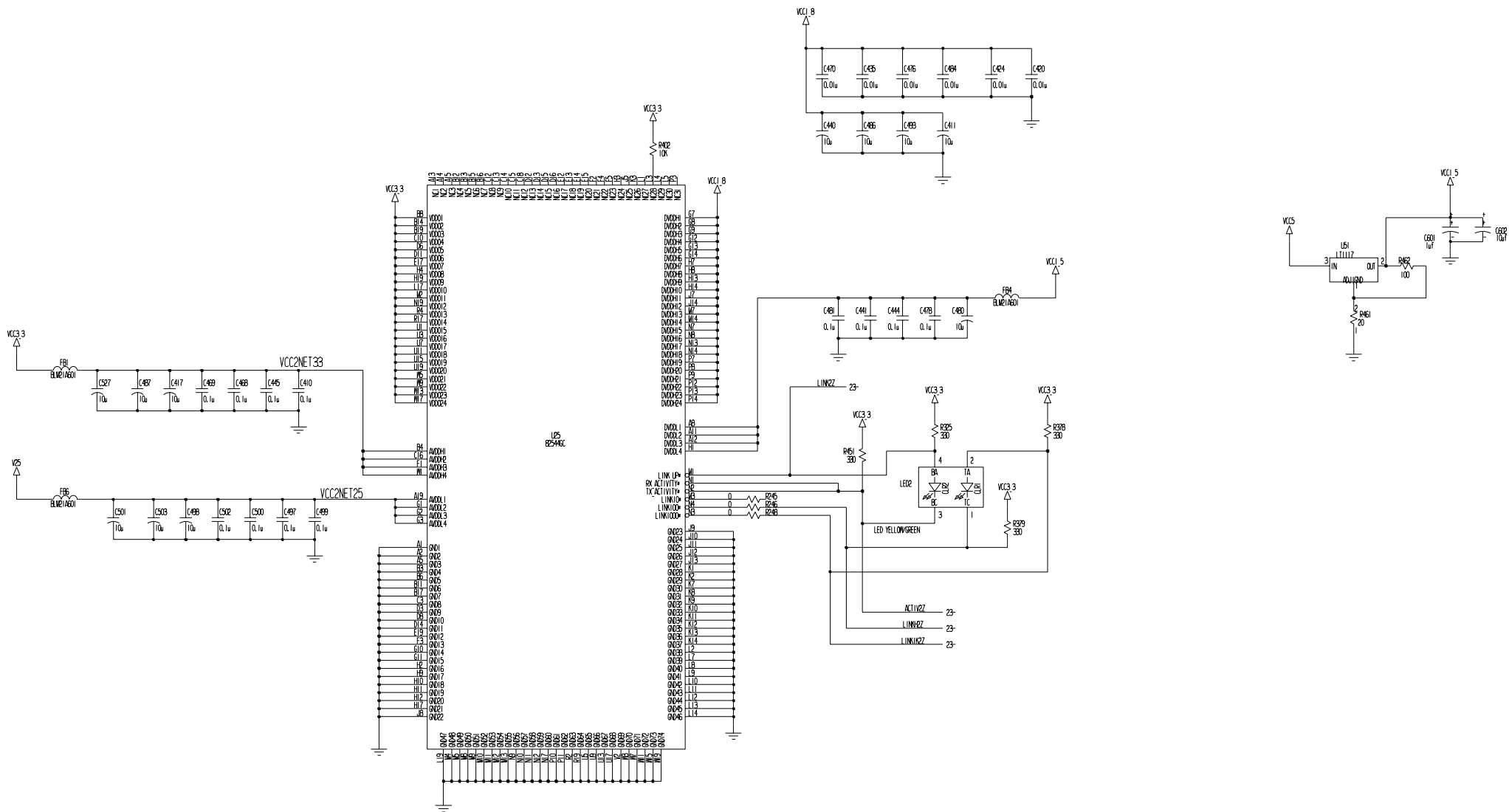
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Date Changed  
Thursday, January 10, 2002

Time  
12:55:42 pm







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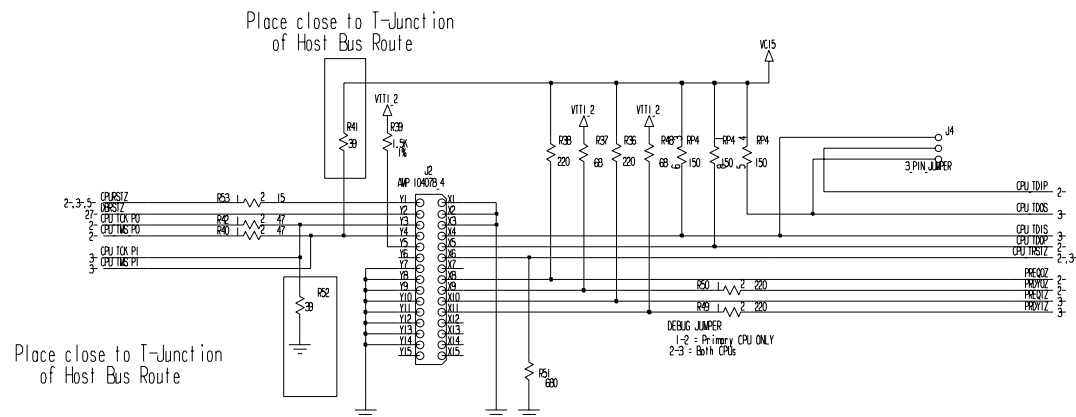
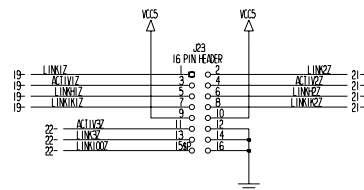
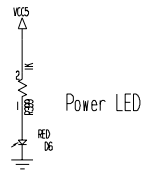
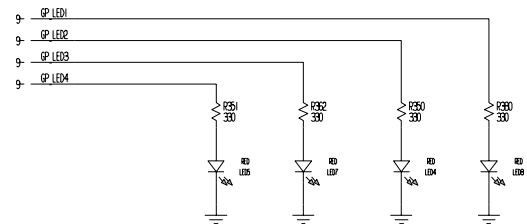
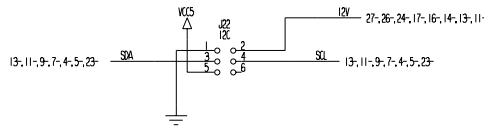
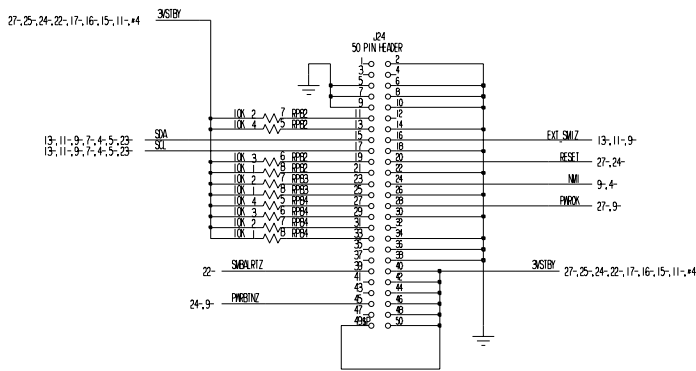
Engineer p.j.v	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v			
R&D CHK	TITLE Intel® Performance Appliance Platform Ethernet 2 Power		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2	Sheet 21 of 33	

Changed by  
p.j.v

Date Changed  
Thursday, January 10, 2002

Time  
12:56:47 pm





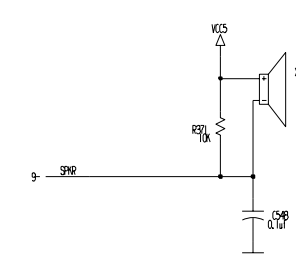
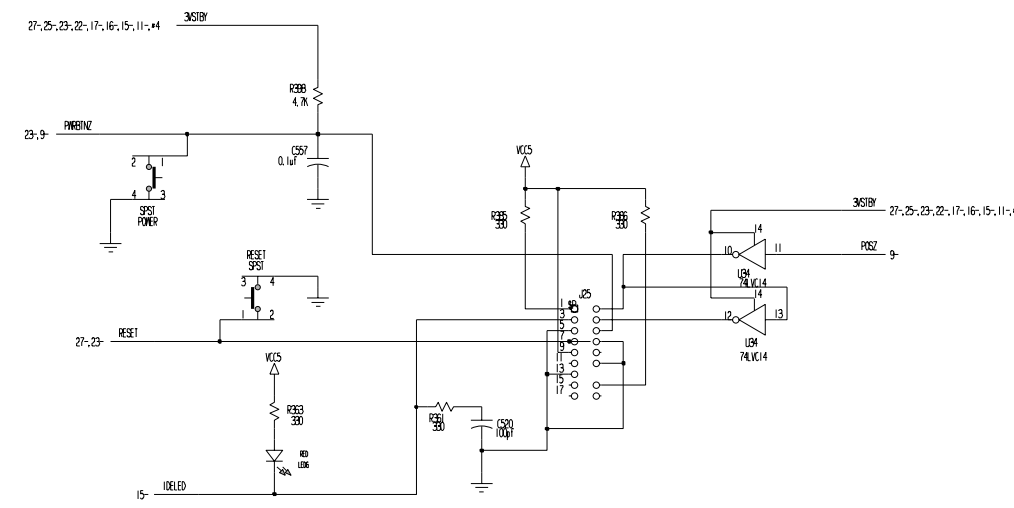
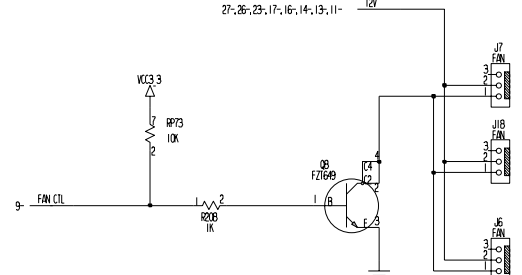
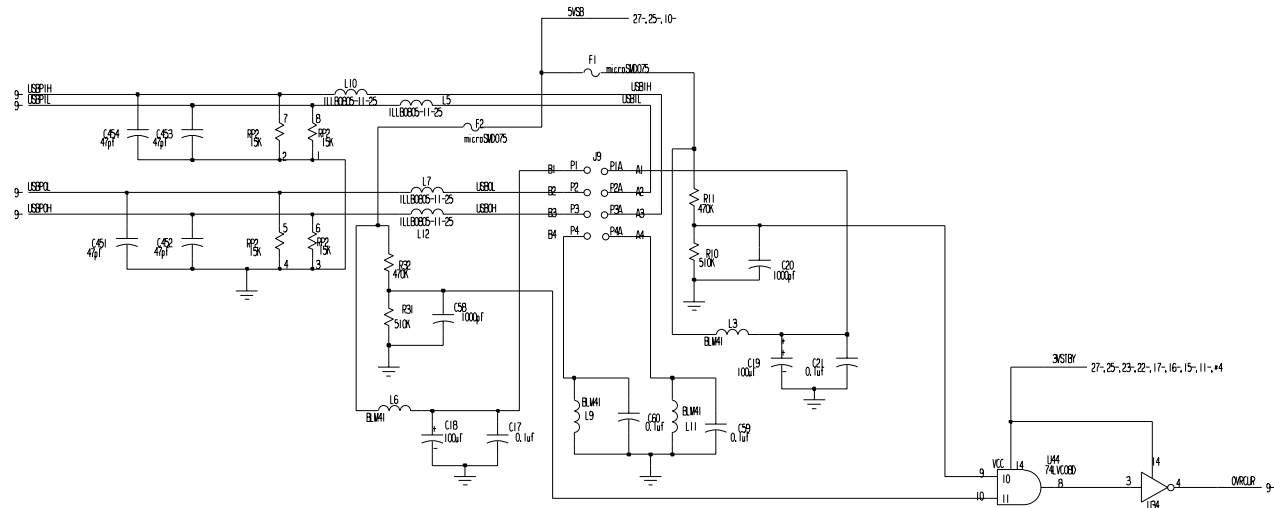
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Engineer p.j.v	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v			
R&D CHK	TITLE		Size D
DOC CTRL CHK	Intel® Performance Appliance Platform		
MFG CTRL CHK	ITP Debug Port & IPMI Connector		
QA CHK	REV 2	Sheet 23 of 33	

Changed by  
p.j.v

Date Changed  
Thursday, January 10, 2002

Time  
12:58:05 pm



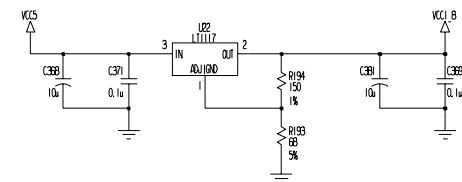
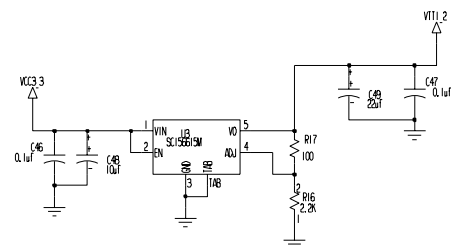
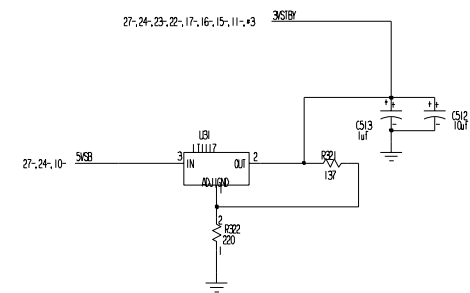
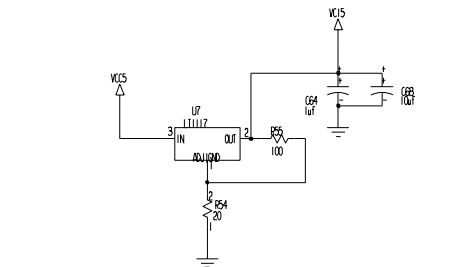
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Engineer p.j.v	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v			
R&D CHK	TITLE		Size D
DOC CTRL CHK	Intel® Performance Appliance Platform		
MFG CTRL CHK	Front Panel, Fan Control and USB		
QA CHK	REV 2	Sheet 24 of 33	

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Thursday, January 10, 2002

Time  
12:58:29 pm



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Engineer p.j.v	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v			
R&D CHK	TITLE  Intel® Performance Appliance Platform  Linear Regulators		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 2		Sheet 25 of 33

Changed by  
p jv

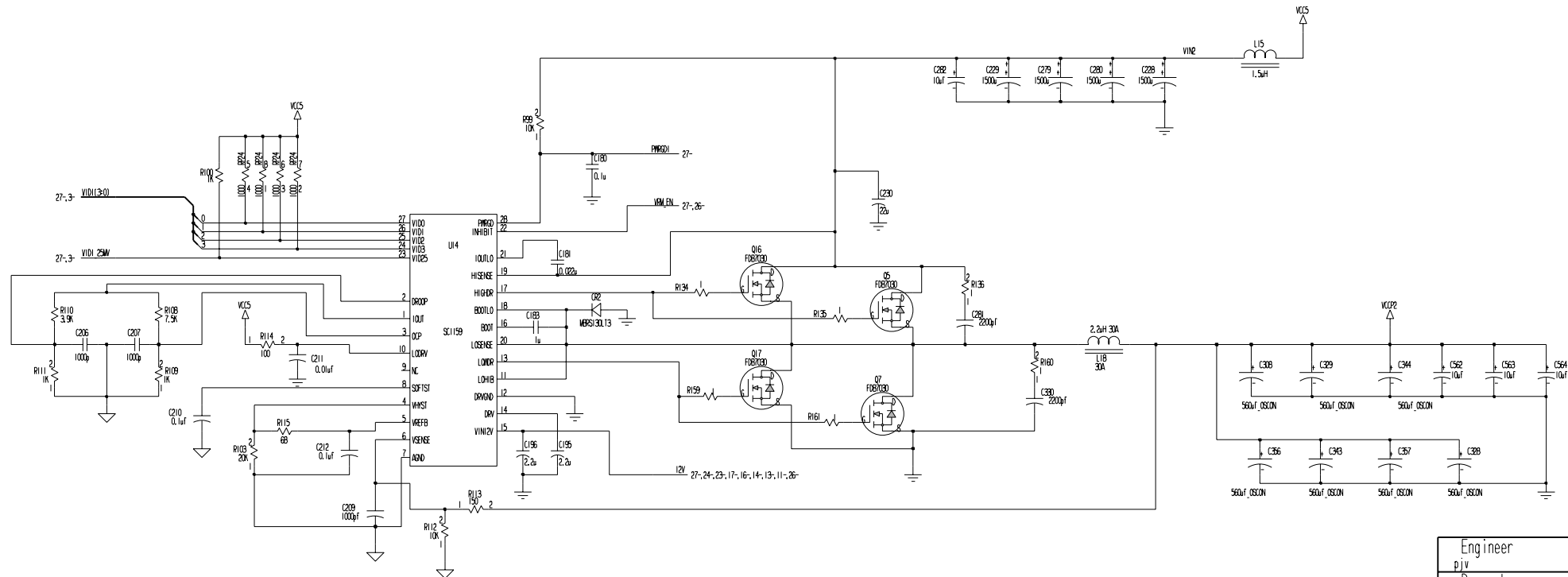
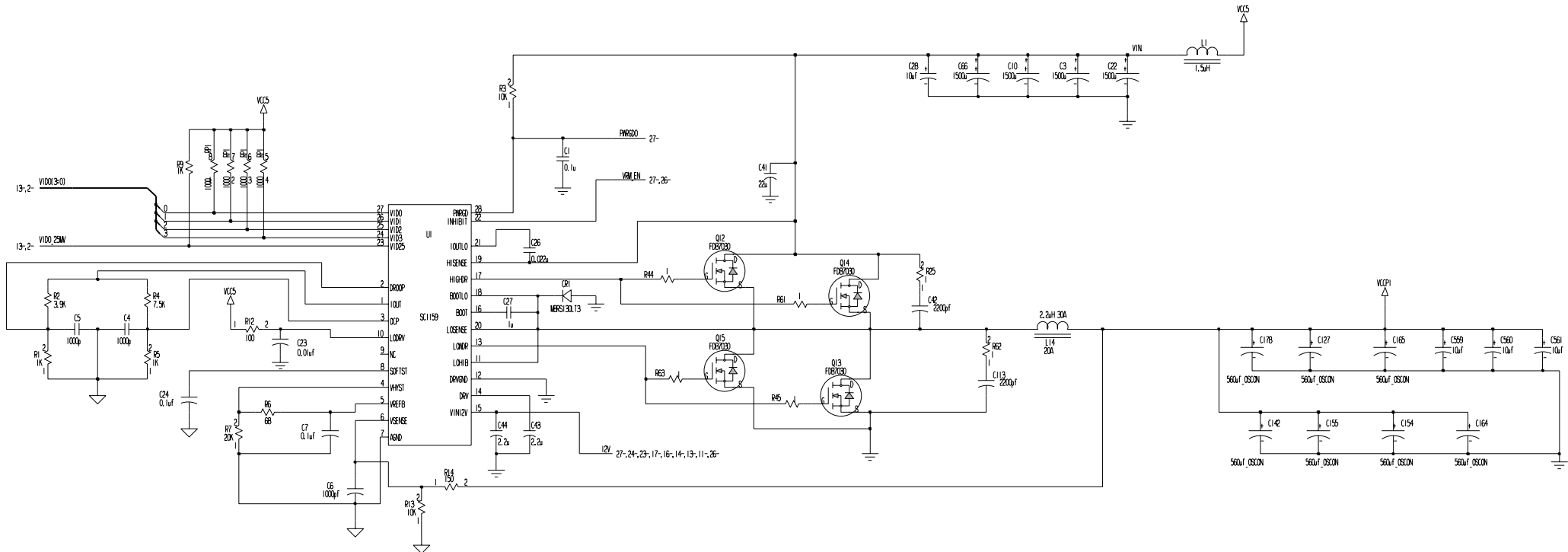
Date Changed  
Thursday, January 10, 2002

Time  
12:58:58 pm

QA CHK

	RE
	2

Sheet 25 of 33



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Engineer p.j.v	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Drawn by p.j.v			
R&D CHK	TITLE		Size D
DOC CTRL CHK	Intel® Performance Appliance Platform		
MFG CTRL CHK	CPU Voltage Regulation Modules (VRM 8.5)		
QA CHK	REV 2	Sheet 26 of 33	

Changed by  
p.j.v

Date Changed  
Thursday, January 10, 2002

Time  
12:59:37 pm





1		2		3		4		5		6		7		8																																																			
<div><div>PCI Device Mapping</div><table><thead><tr><th>Interrupt</th><th>REQ / GNT</th><th>Address</th><th>Device</th></tr></thead><tbody><tr><td></td><td>REQ(0)/GNT(0) REQ(1)/GNT(1)</td><td>AD18</td><td>South Bridge</td></tr><tr><td>2</td><td>REQ(3)/GNT(3)</td><td>AD23</td><td>Ethernet 3 (82550)</td></tr><tr><td>0 1 2 3</td><td>REQ(2)/GNT(2)</td><td>AD22</td><td>SLOT_PCI</td></tr><tr><td>1 2 3 0</td><td>X_REQ(1)/X_GNT(1)</td><td>X_AD26</td><td>SLOT_PCIX</td></tr><tr><td>3</td><td>X_REQ(2)/X_GNT(2)</td><td>X_AD25</td><td>Ethernet 1 (82544)</td></tr><tr><td>1</td><td>X_REQ(3)/X_GNT(3)</td><td>X_AD24</td><td>Ethernet 2 (82544)</td></tr></tbody></table></div> <div><div>I2C Address Mapping</div><table><thead><tr><th>Device</th><th>Address</th></tr></thead><tbody><tr><td>Clock Generator</td><td>D2 - D3H</td></tr><tr><td>EEPROM Freq. Mux</td><td>6E - 6FH</td></tr><tr><td>Northbridge</td><td>COH / Config.</td></tr><tr><td>Southbridge</td><td>40H</td></tr><tr><td>DIMM1</td><td>A0 - A1H</td></tr><tr><td>DIMM2</td><td>A2 - A3H</td></tr><tr><td>DIMM3</td><td>A4 - A5H</td></tr><tr><td>DIMM4</td><td>A6 - A7H</td></tr><tr><td>Super I/O</td><td>4E - 4FH</td></tr><tr><td>Hardware Monitor</td><td>2CH</td></tr></tbody></table></div>																Interrupt	REQ / GNT	Address	Device		REQ(0)/GNT(0) REQ(1)/GNT(1)	AD18	South Bridge	2	REQ(3)/GNT(3)	AD23	Ethernet 3 (82550)	0 1 2 3	REQ(2)/GNT(2)	AD22	SLOT_PCI	1 2 3 0	X_REQ(1)/X_GNT(1)	X_AD26	SLOT_PCIX	3	X_REQ(2)/X_GNT(2)	X_AD25	Ethernet 1 (82544)	1	X_REQ(3)/X_GNT(3)	X_AD24	Ethernet 2 (82544)	Device	Address	Clock Generator	D2 - D3H	EEPROM Freq. Mux	6E - 6FH	Northbridge	COH / Config.	Southbridge	40H	DIMM1	A0 - A1H	DIMM2	A2 - A3H	DIMM3	A4 - A5H	DIMM4	A6 - A7H	Super I/O	4E - 4FH	Hardware Monitor	2CH
Interrupt	REQ / GNT	Address	Device																																																														
	REQ(0)/GNT(0) REQ(1)/GNT(1)	AD18	South Bridge																																																														
2	REQ(3)/GNT(3)	AD23	Ethernet 3 (82550)																																																														
0 1 2 3	REQ(2)/GNT(2)	AD22	SLOT_PCI																																																														
1 2 3 0	X_REQ(1)/X_GNT(1)	X_AD26	SLOT_PCIX																																																														
3	X_REQ(2)/X_GNT(2)	X_AD25	Ethernet 1 (82544)																																																														
1	X_REQ(3)/X_GNT(3)	X_AD24	Ethernet 2 (82544)																																																														
Device	Address																																																																
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Southbridge	40H																																																																
DIMM1	A0 - A1H																																																																
DIMM2	A2 - A3H																																																																
DIMM3	A4 - A5H																																																																
DIMM4	A6 - A7H																																																																
Super I/O	4E - 4FH																																																																
Hardware Monitor	2CH																																																																
<div><div>Voltage Identification</div><table><tbody><tr><td>VCCP1</td><td>+1.45V - Primary CPU Voltage</td></tr><tr><td>VCCP2</td><td>+1.45V - Secondary CPU Voltage</td></tr><tr><td>VCC5</td><td>+5V</td></tr><tr><td>VCC3.3</td><td>+3.3V</td></tr><tr><td>V25</td><td>+2.5V for Northbridge,Soutbridge &amp; DDR Memory</td></tr><tr><td>VTT1_2</td><td>+1.25V for CPU Termination</td></tr><tr><td>VC15</td><td>+1.5V for CPU CMOS Termination</td></tr><tr><td>MVTT</td><td>+1.25V - Memory VTT (Termination)</td></tr><tr><td>M_VREF</td><td>+1.25V - Memory Vref</td></tr><tr><td>3VSTBY</td><td>+3.3V Auxillary Voltage (Standby)</td></tr><tr><td>I2V</td><td>+12V</td></tr><tr><td>2_5VSB</td><td>+2.5V - Battery Voltage for Southbridge</td></tr><tr><td>3VBAT</td><td>+3.3V - Battery Voltage for Devices</td></tr><tr><td>2VBAT</td><td>+2.5V - Battery Voltage for Southbridge Only</td></tr><tr><td>VCC1_8</td><td>+1.8V NIC Voltage</td></tr><tr><td>VCC2_5</td><td>+2.5V NIC Voltage</td></tr><tr><td>VCC1_5</td><td>+1.5V NIC Voltage</td></tr></tbody></table></div> <div><div>THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.</div><div><table><tbody><tr><td>Engineer p.j.v.</td><td colspan="3" rowspan="5">Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226</td><td rowspan="5">TITLE Intel® Performance Appliance Platform PCI &amp; I2C Device Mapping</td><td rowspan="8">Size D</td></tr><tr><td>Drawn by p.j.v.</td></tr><tr><td>R&amp;D CHK</td></tr><tr><td>DOC CTRL CHK</td></tr><tr><td>MFG CTRL CHK</td></tr><tr><td>QA CHK</td><td>REV 2</td><td colspan="2" rowspan="2"></td><td colspan="2" rowspan="2">Sheet 28 of 33</td></tr></tbody></table></div></div>																VCCP1	+1.45V - Primary CPU Voltage	VCCP2	+1.45V - Secondary CPU Voltage	VCC5	+5V	VCC3.3	+3.3V	V25	+2.5V for Northbridge,Soutbridge & DDR Memory	VTT1_2	+1.25V for CPU Termination	VC15	+1.5V for CPU CMOS Termination	MVTT	+1.25V - Memory VTT (Termination)	M_VREF	+1.25V - Memory Vref	3VSTBY	+3.3V Auxillary Voltage (Standby)	I2V	+12V	2_5VSB	+2.5V - Battery Voltage for Southbridge	3VBAT	+3.3V - Battery Voltage for Devices	2VBAT	+2.5V - Battery Voltage for Southbridge Only	VCC1_8	+1.8V NIC Voltage	VCC2_5	+2.5V NIC Voltage	VCC1_5	+1.5V NIC Voltage	Engineer p.j.v.	Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226			TITLE Intel® Performance Appliance Platform PCI & I2C Device Mapping	Size D	Drawn by p.j.v.	R&D CHK	DOC CTRL CHK	MFG CTRL CHK	QA CHK	REV 2			Sheet 28 of 33	
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11-B7		C239 3-E4 C240 3-E5 C241 3-B6 C242 3-E5 C243 3-E5 C244 3-E5 C245 3-E5 C246 3-D4 C247 5-E2 C248 5-E5 C249 5-D4 C250 5-E3 C251 5-E2 C252 5-B6 C253 5-D7 C254 7-E5 C255 7-E1 C256 7-E6 C257 3-E2 C258 3-E5 C259 3-B5 C260 3-B5 C261 6-E3 C262 3-B5 C263 3-D4 C264 3-B5 C265 5-E1 C266 5-E4 C267 5-E2 C268 5-E4 C269 6-E5 C270 5-E4 C271 5-E4 C272 5-E5 C273 6-E2 C274 5-E6 C275 10-E5 C276 5-E2 C277 7-E4 C278 7-E5 C279 26-C5 C280 26-C5 C281 26-B5 C282 26-C5 C283 22-A3 C284 3-E5 C285 3-E5 C286 3-E5 C287 3-E5 C288 3-E5 C289 3-D4 C290 6-E4 C291 6-E4 C292 6-E4 C293 5-E4 C294 6-E3 C295 5-E4 C296 6-E3 C297 10-E5 C298 10-E5 C299 7-E5 C300 4-A4 C301 5-E3 C302 10-E5 C303 10-E5 C304 10-E5 C305 7-E4 C306 7-E4 C307 7-E1 C308 26-B6 C309 3-B2 C310 3-B5 C311 5-E1 C312 3-E4 C313 3-B5 C314 3-B5 C315 3-B4 C316 3-D4 C317 3-B5 C318 3-B5 C319 3-B4 C320 4-A4		C321 10-E5 C322 10-B8 C323 5-E5 C324 5-E4 C325 7-E2 C326 7-E4 C327 7-E2 C328 26-B6 C329 26-B6 C330 26-B5 C331 5-E4 C332 3-E5 C333 5-E2 C334 4-A4 C335 4-A4 C336 4-A4 C337 6-E2 C338 19-A5 C339 5-D7 C340 7-E2 C341 7-E2 C342 7-E5 C343 26-B6 C344 26-B6 C345 6-C3 C346 4-A5 C347 4-A5 C348 12-B8 C349 10-E5 C350 4-B8 C351 5-E2 C352 6-B5 C353 9-E7 C354 7-C3 C355 5-B6 C356 26-B6 C357 26-B6 C358 5-E1 C359 22-B2 C360 22-A3 C361 5-E2 C362 7-E4 C363 17-B2 C364 16-E2 C365 4-B8 C366 10-B3 C367 6-E2 C368 25-C5 C369 25-C6 C370 10-B7 C371 25-C5 C372 6-E5 C373 17-B8 C374 16-E2 C375 5-E4 C376 16-E3 C377 10-E5 C378 10-E5 C379 17-E5 C380 19-A6 C381 25-C6 C382 6-E6 C383 17-B2 C384 10-B3 C385 10-D4 C386 21-B8 C387 10-B7 C388 10-B7 C389 10-B7 C390 10-B6 C391 6-B6 C392 7-B1 C393 5-E1 C394 10-C3 C395 10-C3 C396 10-C3 C397 10-C4 C398 11-B6 C399 11-B6 C400 11-B6 C401 11-B6 C402 10-C3		C403 9-C7 C404 9-C7 C405 6-E6 C406 10-D4 C407 20-A4 C408 10-B3 C409 17-B5 C410 21-B3 C411 21-A6 C412 6-E6 C413 19-A5 C414 19-B8 C415 19-B8 C416 5-E3 C417 21-B8 C418 9-C7 C419 19-A5 C420 21-A6 C421 19-A6 C422 22-C5 C423 19-A6 C424 21-A6 C425 9-C7 C426 9-B6 C427 9-C7 C428 20-C3 C429 5-E4 C430 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17-E5 C620 17-E5 C621 17-E5 C622 17-E5 C623 17-E5 C624 17-E5 C625 17-E5 C626 17-E5 C627 17-E5 C628 17-E5 C629 17-E5 C630 17-E5 C631 17-E5 C632 17-E5 C633 17-E5 C634 17-E5 C635 17-E5 C636 17-E5 C637 17-E5 C638 17-E5 C639 17-E5 C640 17-E5 C641 17-E5 C642 17-E5 C643 17-E5 C644 17-E5 C645 17-E5 C646 17-E5 C647 17-E5 C648 17-E5 C649 17-E5 C650 17-E5 C651 17-E5 C652 17-E5 C653 17-E5 C654 17-E5 C655 17-E5 C656 17-E5 C657 17-E5 C658 17-E5 C659 17-E5 C660 17-E5 C661 17-E5 C662 17-E5 C663 17-E5 C664 17-E5 C665 17-E5 C666 17-E5 C667 17-E5 C668 17-E5 C669 17-E5 C670 17-E5 C671 17-E5 C672 17-E5		C673 7-E2 C674 12-B6 C675 17-B6 C676 17-B2 C677 17-B6 C678 9-C8 C679 7-B1 C680 7-B1 C681 11-A3 C682 9-C7 C683 6-E3 C684 7-B1 C685 6-E6 C686 6-E2 C687 12-B2 C688 6-E2 C689 10-E5 C690 27-D1 C691 11-A3 C692 9-C7 C693 6-C4 C694 6-E3 C695 9-C8 C696 9-C4 C697 6-E6 C698 27-D1 C699 11-A3 C700 6-E6 C701 10-E4 C702 7-E4 C703 7-E3 C704 27-E2 C705 17-B3 C706 12-B6 C707 17-B3 C708 6-E6 C709 6-E6 C710 11-A4 C711 17-B3 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J10 10-C7 J11 6-E2 J12 4-D4 J13 6-B3 J14 15-B5 J15 15-B5 J16 13-D4 J17 11-B7 J17 11-B7 J18 24-D4 J19 13-B5 J20 12-B5 J21 23-C9 J22 23-B3 J23 23-E3 J24 23-B3 J25 24-C7 J26 11-B5 J27 11-E4 REFDES SH-ZONE R1 26-B2 R2 26-B2 R3 26-A4 R4 26-B2 R5 26-B2 R6 26-B3 R7 26-B3 R8 26-B2 R9 26-B2 R10 24-B3 R11 24-B3 R12 26-B3 R13 26-C3 R14 26-B3 R16 25-C3 R17 25-C3 R18 14-C6 R19 14-C2 R20 14-C2 R21 14-C2 R22 14-C2 R23 14-C2 R25 26-B5 R26 2-A6 R27 2-D4 R28 14-C6 R29 14-C5 R30 14-B2		L21 11-B6 L22 11-C7 L23 11-B6 L24 11-B6 L25 10-C4 L26 11-C6 L27 11-C6 L28 22-B4 REFDES SH-ZONE LED1 19-C6 LED2 21-C6 LED3 22-D5 LED4 23-D3 LED5 23-D3 LED6 24-C6 LED7 23-D3 LED8 23-D4 REFDES SH-ZONE OPT1 9-C2 REFDES SH-ZONE POWER 24-B6 REFDES SH-ZONE O1 2-B5 O2 14-C6 O3 14-C6 O4 3-B5 O5 26-D4 O6 4-C3 O7 26-B4 O8 24-B3 O9 9-B5 O10 12-B4 O11 12-B3 O12 26-B4 O13 26-B5 O14 26-B5 O15 26-B4 O16 26-D4 O17 26-D4 REFDES SH-ZONE R1 26-B2 R2 26-B2 R3 26-A4 R4 26-B2 R5 26-B2 R6 26-B3 R7 26-B3 R8 26-B2 R9 26-B2 R10 24-B3 R11 24-B3 R12 26-B3 R13 26-C3 R14 26-B3 R16 25-C3 R17 25-C3 R18 14-C6 R19 14-C2 R20 14-C2 R21 14-C2 R22 14-C2 R23 14-C2 R25 26-B5 R26 2-A6 R27 2-D4 R28 14-C6 R29 14-C5 R30 14-B2		REFDES SH	

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R119 5-C2	R202 6-D3	R289 10-D7	R371 24-D6	R456 8-C5	R527 8-B2	R647 16-A6	R720 9-B7	T18 9-C3	U18 4-C4						
R120 5-A6	R203 17-A7	R290 10-C7	R372 11-D4	R457 8-B6	R528 8-C7	R647 16-C6	R721 9-B7	T19 18-C2	U20 6-B3						
R121 5-A6	R204 17-A7	R291 10-C6	R373 11-D4	R458 8-C5	R529 8-C7	R647 16-A6	R721 15-B4	T20 18-C5	U21 6-B2						
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R123 3-E1	R206 15-C3	R293 15-B6	R375 11-B3	R460 8-C5	R531 8-C5	R648 5-A7	R722 15-C4	T22 20-C5	U23 4-B5						
R124 3-D1	R207 11-B6	R294 15-C4	R376 19-C6	R461 8-C5	R532 8-B2	R648 5-A8	R722 15-C4	T23 20-C2	U24 9-B3						
R125 5-C2	R208 24-D3	R295 15-B6	R377 19-C6	R462 8-C5	R533 8-B2	R648 5-A8	R722 15-C4	T24 9-A3	U24 10-C3						
R127 3-E1	R209 9-C4	R296 20-D7	R378 21-B6	R463 8-C5	R534 8-B2	R649 5-A7	R723 12-B5	T25 9-A3	U25 20-C2						
R128 3-D2	R210 17-B7	R297 21-B5	R379 21-C6	R464 8-C5	R535 8-B2	R649 5-A7	R723 9-B3	T26 18-C5	U25 20-C5						
R129 3-E2	R211 4-B5	R298 13-B5	R380 23-C4	R465 8-C5	R536 8-C4	R649 5-A7	R723 9-B3	T27 9-B4	U26 21-C4						
R130 17-B7	R212 11-B6	R299 13-B5	R381 22-C5	R466 8-B6	R537 8-C4	R649 5-A7	R723 12-B5	T28 9-B4	U26 13-B4						
R131 17-B7	R213 18-C3	R300 15-B4	R382 22-C5	R467 8-B6	R538 8-C4	R649 5-A8	R724 15-B4	T29 9-B3	U27 18-C2						
R132 17-B7	R214 17-A7	R301 18-C5	R383 22-C5	R468 8-C2	R539 8-C4	R650 5-A7	R724 15-B4	T30 18-C5	U27 18-C5						
R133 5-C2	R215 9-B5	R302 18-C5	R384 22-D3	R469 8-C2	R540 8-C5	R650 5-A7	R724 15-B4	T31 20-B5	U27 19-D4						
R134 26-D4	R216 17-B7	R303 18-B5	R385 24-C7	R470 8-C2	R541 8-B7	R650 5-A7	R725 15-D4	T32 18-B5	U28 10-C6						
R135 26-D4	R217 11-C6	R304 18-C5	R386 24-C7	R471 8-C2	R542 8-C5	R650 5-A7	R725 15-D4	T33 18-B5	U29 18-B4						
R136 26-D5	R218 11-C6	R305 18-C6	R387 11-D4	R472 8-C5	R543 8-B7	R651 5-A7	R725 15-C4	T34 20-C5	U30 10-B6						
R137 3-D4	R219 18-B5	R306 18-C6	R388 11-D4	R473 8-C5	R544 8-B7	R651 5-A7	R726 9-C3	T35 20-C5	U31 25-B5						
R138 3-D4	R220 20-C3	R307 18-C5	R389 11-D4	R474 8-C5	R545 8-B7	R651 5-A7	R726 9-C3	T36 20-B5	U32 27-D4						
R139 4-C5	R221 20-C3	R308 18-C5	R390 27-A5	R475 8-C5	R546 8-B7	R652 5-A7	R726 9-B3	T37 11-C3	U32 4-B3						
R140 4-C4	R222 16-C6	R309 18-C5	R391 22-C5	R476 8-C5	R547 8-B7	R652 5-A7	R726 9-C3	T38 11-C3	U32 27-B7						
R141 4-C5	R223 20-C3	R310 18-C5	R392 22-D3	R477 8-C5	R548 8-B7	R652 5-A7	R727 9-B3	T39 11-C3	U32 27-B3						
R142 4-C5	R224 20-B3	R311 18-C5	R393 22-E3	R478 8-C5	R549 8-B7	R652 5-A7	R727 9-B3	T40 11-C3	U32 27-B3						
R143 17-B7	R225 9-B5	R312 20-B5	R394 22-D3	R479 8-B6	R550 8-B7	R653 5-A7	R727 9-B3	T41 11-C3	U33 20-B5						
R144 4-C3	R226 15-A4	R313 20-B6	R395 22-E3	R480 8-B7	R551 8-B7	R653 5-A7	R727 9-B3	T42 11-B3	U34 4-D4						
R145 4-C2	R227 13-D4	R314 20-B6	R396 22-E2	R481 8-B7	R552 8-C4	R653 5-A7	R727 9-B3	T43 22-C5	U34 24-C4						
R146 3-D2	R228 15-B4	R315 20-B6	R397 22-E3	R482 8-B7	R553 8-C4	R653 5-A7	R727 9-B3	T44 22-C5	U34 4-B3						
R147 3-D4	R229 15-D4	R316 20-B6	R398 24-B6	R483 8-B7	R554 8-C4	R654 5-A7	R727 9-B3	T45 22-C5	U34 24-C7						
R148 4-C4	R230 13-B4	R317 20-B6	R399 23-D4	R484 8-B7	R555 8-C4	R654 5-A7	R727 9-B3	T46 22-C5	U34 27-B6						
R149 4-C4	R231 13-B5	R318 20-B6	R400 16-C3	R485 8-B7	R556 8-C5	R654 5-A7	R727 9-B3	T47 15-B4	U34 24-C7						
R150 4-B3	R232 16-B6	R319 20-B6	R401 19-B5	R486 8-B7	R557 8-C5	R654 5-A7	R727 9-B3	T48 15-B4	U35 27-B7						
R151 4-C3	R233 18-B4	R320 20-C6	R402 21-A4	R487 8-B7	R558 8-B7	R655 5-A7	R727 9-B3	T49 15-B4	U35 27-B2						
R152 4-B5	R234 18-C3	R321 20-C6	R403 4-B3	R488 8-B7	R559 8-B7	R655 5-A7	R727 9-B3	T50 15-B4	U35 27-B2						
R153 4-B5	R235 18-B4	R322 20-C6	R404 16-B6	R489 8-C5	R560 8-C5	R655 5-A7	R727 9-B3	T51 11-C4	U35 27-B7						
R154 4-B3	R236 18-C2	R323 25-B6	R405 16-B6	R490 8-C5	R561 8-C5	R656 5-A7	R727 9-B3	T52 11-C4	U36 27-B2						
R155 4-B5	R237 18-C3	R324 25-B5	R406 16-B6	R491 8-B4	R562 8-B7	R656 5-A7	R727 9-B3	T53 11-C4	U36 27-B2						
R156 4-B5	R238 19-C5	R325 27-B3	R407 27-C6	R492 8-C2	R563 8-B7	R656 5-A7	R727 9-B3	T54 22-B3	U36 15-C4						
R157 4-B5	R239 19-C5	R326 19-C6	R408 22-E3	R493 8-C2	R564 8-B7	R656 5-A7	R727 9-B3	T55 12-B4	U36 15-C4						
R158 4-B5	R240 18-B3	R327 21-B6	R409 20-B5	R494 8-C2	R565 8-C4	R656 5-A7	R727 9-B3	T56 12-B4	U37 27-E1						
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R160 26-D5	R242 20-C4	R329 20-D7	R411 19-C5	R496 8-C5	R567 8-C4	R658 9-B7	R727 9-B3	T58 12-B4	U37 27-D1						
R161 26-D4	R243 20-C4	R330 4-D3	R412 21-C5	R497 8-C5	R568 17-C7	R658 9-B7	R727 9-B3	T59 23-A2	U37 27-D1						
R162 4-C4	R244 20-C4	R331 18-B5	R413 9-A4	R498 8-B7	R569 17-C7	R658 9-B7	R727 9-B3	T60 23-A2	U38 27-D4						
R163 2-D2	R245 21-C5	R332 18-B5	R414 9-A4	R499 8-B7	R570 17-C7	R659 17-C7	R727 9-B3	T61 23-A2	U38 27-C5						
R164 4-B5	R246 21-C5	R333 18-B5	R415 9-A4	R500 8-B7	R571 17-C7	R659 17-C7	R727 9-B3	T62 23-A2	U38 27-B5						
R165 4-C6	R247 20-C3	R334 18-C6	R416 9-A4	R501 8-B7	R572 17-C7	R659 17-C7	R727 9-B3	T63 23-A2	U39 27-D4						
R166 4-B5	R248 21-C5	R335 15-C4	R417 21-B7	R502 8-C5	R573 17-C7	R659 17-C7	R727 9-B3	T64 23-A2	U39 11-B5						
R167 4-C6	R249 16-B6	R336 10-B6	R418 21-B7	R503 8-B5	R574 17-C7	R660 9-B3	R727 9-B3	T65 23-A2	U40 11-B3						
R168 4-C5	R250 9-B5	R337 22-C5	R419 27-C6	R504 8-B7	R575 8-B7	R660 9									

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